REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed July 31, 2009. The Examiner is thanked for the thorough examination of the present application. Upon entry of this response, claims 1-5, 13, 16-24, 32, 33, and 35-38 are pending in the present application. Applicants respectfully request consideration of the following remarks contained herein. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

I. Summary of Telephone Interview with Examiner

Applicants wish to thank Examiner Do for the time spent with Applicants' representative Jeffrey Hsu (Registration No. 63,063) during a telephone interview conducted on October 29, 2009 regarding the above-identified Office Action. During the interview, a general agreement was reached that the cited art of record does not disclose an "overriding" feature, as reflected in the proposed amendments discussed. In this regard, the Examiner indicated that Applicants' proposed amendments would be sufficient to overcome the rejections indicated by the Office Action. Applicants submit that the comments and amendments set forth herein are consistent with those raised during the interview.

II. Response to Claim Rejections Under 35 U.S.C. § 103

In the current Office Action, claims 1-5, 13, 20-24, and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Okumura et al.* (U.S. Patent No. 5,726,923 hereinafter "*Okumura*") in view of *MicInnis et al.* (U.S. Pub. No. 2003/0185305 hereinafter "*MicInnis*"). Claims 16-19 and 35-38 are rejected under 35 U.S.C. 103(a)

as being unpatentable over *Okumura* in view of *MacInnis* in further view of the admitted prior art. Applicants respectfully request consideration of the following remarks.

A. Claims 1-5

Applicants respectfully submit that independent claim 1 patently defines over *Okumura* in view of *MacInnis* for at least the reason that the combination fails to disclose, teach, or suggest the features emphasized below in claim 1.

Claim 1, as amended, recites:

> 1. A communications processor for implementing scheduling processes and reducing the processing effort for determining a minimum value of a plurality of values stored in source registers and determining an index value of a source register having the minimum value, the communications processor comprising:
> a destination register;
> a first source register storing a first value, wherein the first source register comprises S bits, and wherein the first value comprises N lower bits of the first source register;
> a second source register storing a second value, wherein the second source register comprises S bits, and wherein the second value comprises N lower bits of the second source register;
> means for comparing the first value stored in the first source register with the second value stored in the second source register, wherein the first source register and the second source register each include an active status bit to indicate a status of the respective register;
> means for storing the first value in the destination register when the first value is less than or equal to the second value;
> means for concatenating the index value with the second value into a concatenated value and storing the concatenated value in the destination register when the second value is less than the first value; and
> ***means for overriding a result from the comparing means based on the active status bits of the first and second source registers***, wherein the index value is stored in an upper (S-N) bits of the concatenated value and the second value stored in the N lower bits of the concatenated value.

(Emphasis added). For "active status bits" in claim 1, the Office Action now cites the secondary *MacInnis* reference in acknowledging that *Okumura* fails to disclose or

suggest these features. Specifically, on pages 3-4, the Office Action cites paragraphs [0038] and [0042] in *MacInnis* in alleging that *MacInnis* discloses the "active status bit" corresponding to the first and second source registers in claim 1. Applicants respectfully traverse the rejection. First, *MacInnis* is directed to systems and methods for communicating between modules in a decoding system. Paragraph [0038] describes a pipeline in which decoding is performed by issuing commands to each hardware accelerator module for each pipeline stage. Namely, each hardware module 306, 308, 309, 310, 312, 313, 315 shown in FIG. 3 performs a task. *MacInnis* teaches that each hardware module includes a status register that indicates whether a corresponding hardware module is active or inactive. *MacInnis* further discloses that the status register may also indicate the internal state of the hardware accelerator at a specific point during the processing stage of the hardware accelerator. Applicants respectfully submit that the status register taught by *MacInnis* is not equivalent to the "active status bit" in claim 1. Claim 1 explicitly defines that the first source register and the second source register each include an active status bit to indicate a status of that respective register, and not of a corresponding hardware module. Applicants have chosen the element "active status bit" to indicate a status of the respective register which it is a part of and respectfully submit that a broadest reasonable interpretation of this element would not read on a status of a hardware module. *See* MPEP 2111, The Patent and Trademark Office ("PTO") determines the scope of claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction "in light of the specification as it would be interpreted

by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364[, 70 USPQ2d 1827] (Fed. Cir. 2004).

Notwithstanding, in an effort to advance prosecution, Applicants have amended claim 1 to now recite "means for overriding." Support for the feature above can be found in at least page 24, lines 19 to page 25, line 2 of the specification. Applicants respectfully submit that neither *Okumura* nor *MacInnis* discloses this feature. As described in the specification, for some embodiments, an active module determines if one or more of the active bits are set to "inactive." If one of the values is inactive, the active module selects the active value as the minimum and provides a signal to the MUX indicating the active value as the minimum value. If both values are inactive, the active module selects the first value and provides a signal indicating the value as the minimum regardless of the actual relation between the values. In this regard, the signal indicating the minimum provided by the active module may conflict with the signals provided by the overflow module and/or the comparator. Accordingly, in one embodiment, the signal from the active module overrides the signals from both the comparator and the overflow module.

For "active status bits," the Office Action acknowledges that *Okumura* fails to disclose this feature but alleges that the status bits relating to hardware modules in the *MacInnis* reference reads on this feature. Even assuming, for the sake of argument, that *MacInnis* discloses the active status bits in claim 1, *MacInnis* fails to disclose or suggest overriding the comparing step. Furthermore, *Okumura* fails to address this deficiency.

Accordingly, Applicants respectfully submit that independent claim 1 patently defines over *Okumura* in view of *MacInnis*. Furthermore, Applicants submit that dependent claims 2-5 are allowable for at least the reason that these claims depend from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

B. Claim 13

Applicants respectfully submit that independent claim 13 patently defines over *Okumura* in view of *MacInnis* for at least the reason that the combination fails to disclose, teach, or suggest the features emphasized below in claim 13.

Claim 13, as amended, recites:

> 13. A method implemented as instructions for manipulating a network processor for implementing scheduling processes and reducing a number of network processor cycles for determining a minimum value and a corresponding index value of a plurality of source registers of the network processor, the method comprising the steps of:
> . . .
> ***examining active status bits comprising the least significant bits of the values in the source register and in the destination register;***
> ***based on the active status bits, overriding the comparing step and selecting an active value as a current minimum*** . . .

(Emphasis added). Applicants submit that the features emphasized above in claim 13 embody substantive features that are similar to the defining features of claim 1 discussed above. Namely, claim 13 now recites the steps of "examining active status bits" that comprises the least significant bits of the values being compared. Claim 13 further defines that based on these active status bits, the result from the comparison of these values may be overridden. As described in the specification, this may occur, for

example, if both values are inactive. As discussed above for claim 1, neither *Okumura* nor *MacInnis* discloses or suggests this feature. Claim 13 further recites "based on the active status bits, . . . selecting an active value as a current minimum." Applicants respectfully submit that again, neither *Okumura* nor *MacInnis* discloses or suggests this feature. In view of the foregoing, Applicants respectfully request that the rejection be withdrawn.

C. Claims 17-24, 32-33, 36-38

As independent claims 17, 20, 32, and 36 now embody substantive features similar to those discussed above for claims 1 and 13, Applicants respectfully request that the rejections be withdrawn for reasons similar to those discussed above. Applicants submit that dependent claims 18-19, 21-24, 33, and 37-38 are allowable for at least the reason that these claims depend from allowable independent claims.

D. Claim 16

Claim 16 stands rejected under 35 U.S.C. §103(a) as being unpatentable over *Okumura* in view of *MacInnis* in further view of *admitted prior art*. As set forth above, Applicants submit that independent claim 13, from which claim 16 depends, respectively, is patentable over *Okumura* in view of *MacInnis*. Furthermore, *admitted prior art* fails to address the deficiencies expressed above for *Okumura* in view of *MacInnis*. As such, Applicants submit that independent claim 13 is patentable over the combination of *Okumura* in view of *MacInnis* in further view of *admitted prior art*. Accordingly, dependent claim 16 is allowable for at least the reason that this claim depends from an allowable independent claim.

E. Claim 35

Claim 35 stands rejected under 35 U.S.C. §103(a) as being unpatentable over *Okumura* in view of *MacInnis* in further view of *admitted prior art*. As set forth above, Applicants submit that independent claim 32, from which claim 35 depends, respectively, is patentable over *Okumura* in view of *MacInnis*. Furthermore, *admitted prior art* fails to address the deficiencies expressed above for *Okumura* in view of *MacInnis*. As such, Applicants submit that independent claim 32 is patentable over the combination of *Okumura* in view of *MacInnis* in further view of *admitted prior art*. Accordingly, dependent claim 35 is allowable for at least the reason that this claim depends from an allowable independent claim.

CONCLUSION

Applicants respectfully submit that all pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephone conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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